



A Review on multithreading processes and threads in multiple cores CPU

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ABSTRACT: The objective of our research is to analyze job handling process of CPU in different circumstances. Here we would analyze how CPU reacts in case of single task & in case when it switches among multiple tasks & how multiple task are managed as thread within a multi-core

processor to execute multiple processes or threads concurrently, appropriately supported by operating system. This approach differs from multiprocessing, as with multithreading processes & threads have to share resources of a single or multiple cores: computing units, CPU caches, & translation lookaside buffer. A scheduler may aim at one of several goals, for example, maximizing *throughput*, minimizing *response time* or minimizing *latency*, maximizing *fairness* (equal CPU time to each process, or more generally appropriate times according to priority & workload of each process). All these goals often conflict thus a scheduler would implement a suitable compromise. Preference is given to any one of concerns mentioned above, depending upon user's needs & objectives.



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[1] INTRODUCTION

CPU is electronic circuitry within a computer that carries out instructions of a computer program by performing basic arithmetic, logical, control & input/output (I/O) operations specified by instructions. term has been used in computer industry at least since early 1960s. Traditionally, term CPU refers to a processor, more specifically to its processing unit & control unit (CU), distinguishing these core elements of a computer from external components such as main memory & I/O circuitry.

The form, design & implementation of CPUs have changed over course of their history, but their fundamental operation remains almost unchanged. Principal components of a CPU include arithmetic logic unit that performs arithmetic & logic

operations, processor registers that supply operands to ALU & store results of ALU operations, & a control unit that fetches instructions from memory & executes them by directing coordinated operations of ALU, registers & other components.

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