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Power Comparison Of Cmos And Full Adder Circuits

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ABSTRACT

Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems the adder lies in the critical path that determines the overall performance of the system. In this paper conventional complementary metal oxide semiconductor (CMOS) and different types of full adder circuits are analyzed in terms of power and delay. A metric to evaluate full adder circuit performance is power delay product (PDP). The driving capability of full adder is very important, because, full adders are mostly used in cascade configuration, where output of one provides the input for others. If full adders lack driving capability then it requires additional buffer which consequently increases the power dissipation.

KEYWORDS

Low-power, CMOS, Full adder, Pass transistor logic, CMOS Transmission gate, Static Energy Recovery Full adder, Adder9A, Adder9B, channel length, delay.

INTRODUCTION

Power minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation and it can lead to reliability and IC packaging problems.