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Analysis Of Low Power Techniques For VLSI Circuit

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Abstract:-This paper, presents a concept of the power optimization theory approach , the estimation techniques and Power consumption is very important issue in VLSI circuit in recent days and power dissipation has become concern for VLSI circuit designers with increase in number of chip. According to MOORE'S in every decade the number of chip is double. So power dissipation is became top challenge in ITRS report roadmap for semiconductor. Speed is second key factor. With advancement of technology everyone wants high speed devices with long power backup. But static and dynamic leakage current results in higher leakage power which reduces the power backup of portable devices.

The main objective of dissertation is to reduce the power consumption of the circuit by using different design techniques. These techniques are sleep, stack, sleep keeper and leakage feedback technique. All these techniques are used for XNOR gate and 1-bit full adder.

A 28T 1-bit full adder is designed on cadence using 180nm technology using all techniques and analyzed the leakage power for the circuit. An 8T XNOR gate also designed on 180nm technology by using all above techniques and leakage power is analyzed. Delay, which reduces the speed of circuit is also analyzed for all above maintained technique.

Introduction:-Power consumption is very important issue in VLSI circuit in recent days. With increase in number of transistors in VLSI circuit we need devices which have lesser power consumption and short delay. But power consumption and delay are contradictory to each other. As supply voltage is lowered to reduce power dissipation, threshold voltage is also lowers to maintain performance of circuit. So for better performance of circuit, it is essential to have smaller threshold voltage